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Do you need MEV PCIe remote update on Cyclone GX FPGA?

Would you like to be able to update your Altera FPGA PCIe card design without having to return the device to the factory?

Would you like this Remote Update solution to already have been done for you, leaving you only to worry about implementing your user logic?

MEV Remote System Update solution (MEV RSU) is a simple way to use Altera's remote update system to deploy new solutions. You are probably using the Cyclone FPGA to implement your own PCIe card solution. This is likely to be a custom industrial solution which may need to be revised, upgraded and/ or bug fixed after the cards have been deployed. This normally means returning the card back to the factory to update its program via the programming header. MEV RSU means you or your end user can update the card firmware in situ without returning the card to base with simple to use tools.

What does it work on?

MEV RSU offers a cost effective, out of the box remote update solution for Altera Cyclone IV GX and Cyclone V GX PCIe solutions.

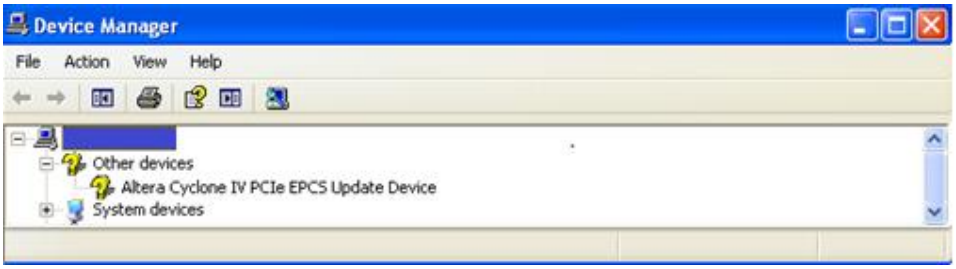
Supporting

- Hard IP PCI express (PCIe) devices on the Cyclone IV or V GX?
- EPCS flash to store the FPGA firmware.
- Windows drivers, API and applications.

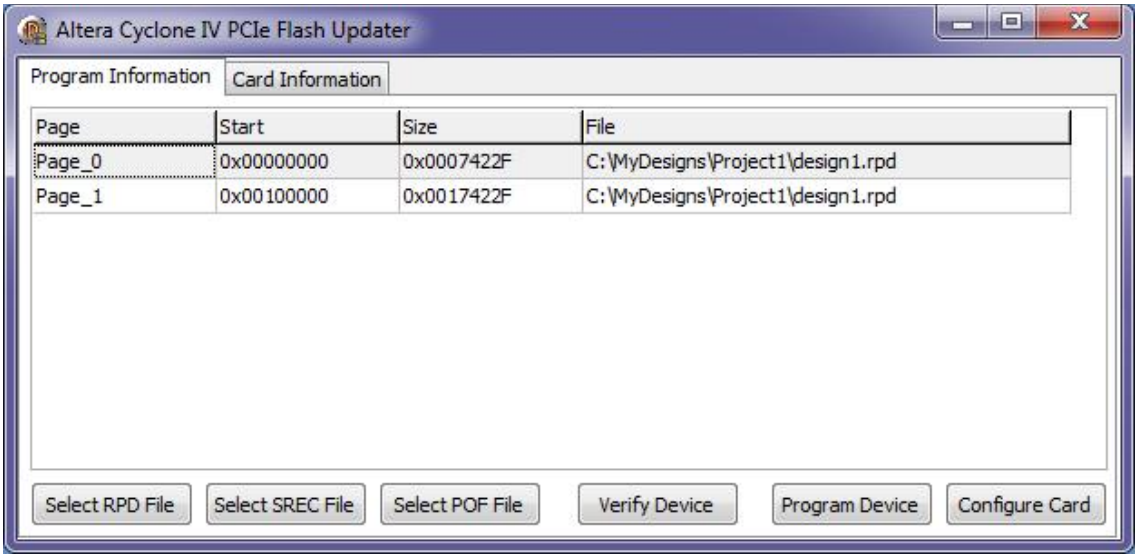
How do you use it?

When it is correctly deployed you will have computer that boots with your user device and will not see MEV RSU at all.

However the PCIe card has been deployed with a dual personality and you can force it to appear as a "MEV Altera Cyclone IV PCIe EPCS update device" if you wish by fitting a jumper or writing a predefined register location via the Cyclone IV updater library API.



MEV provide a Windows application that talks to the "Altera Cyclone IV PCIe EPCS update device" and allows the user image to be updated in EPCS flash. There is an SDK for this interface too so you can write your own applications.



If the update fails then the device will failsafe and the card will still appear as an "Altera Cyclone IV PCIe EPCS update device".

How do you Deploy it?

MEV RSU builds on Altera's Remote Update technology. To deploy MEV RSU you first need to make a programming files for the EPCS flash that contain a factory default image containing MEV RSU and the MEV Altera Cyclone IV PCIe EPCS update device. You create this file in both JIC and POF formats.

Program the EPCS with the JIC and power cycle the system. The card will now boot up as an Altera Cyclone PCIe EPCS Updater device.

Generate your user FPGA logic, making sure it is in remote configuration mode. Once you have a logic design you can create an “Update POF file” that calls in the original POF and your new user logic. This update POF can then be used to overwrite the user flash area using the supplied Cyclone Update application.

What is supplied with it?

MEV RSU solution builds on Altera’s remote update technology to provide a standard, proven fully featured update solution for the Altera Cyclone V GX FPGA PCIe designs for use in Windows environment.

MEV supply

- A standard factory remote update image as EPCS flash or as an IP block
- A standard Altera Cyclone IV or V GX “MEV Altera Cyclone IV PCIe EPCS update” device
- A Windows XP Driver and Logoed Windows 7 (32/64) Driver for the “MEV Altera Cyclone IV PCIe EPCS update” device.
- A Windows user application to allow a new user imaged to be stored in EPCS flash
- A software development kit (SDK) so that a custom upgrade applications can be developed.
- MEV’s reference design generic driver and SDK for the example user images.
- Simple API interface to allow the PCIe card to be switched between being your User Device or the “MEV Altera Cyclone IV PCIe EPCS update” device.

Although the out of the box solution is not currently supported in Linux, with over 10 years’ experience developing embedded Linux solutions we would be able to provide fully a featured device driver and application for Linux operating systems if required for additional cost.

Where Can I Buy It?

You can buy it from MEV web site www.mev.co.uk

FAQ

What are the advantages?

MEV remote system update solution for Cyclone IV and V is proven, fully featured technology that is available now.

MEV's RSU for Cyclone IV GX / V GX based PCIe devices is a mechanism for updating your FPGA firmware via PC software over the PCIe interface using an out of the box driver and application instead of having to return the device to the factory to be reprogrammed. How does it do this? The PCIe card is given a dual personality, normally it appears to be your PCIe device but it can be forced to be a "MEV Altera Cyclone IV PCIe EPCS update device" by programming a register or fitting a jumper.

So it allows you to include a remote update facility without incurring the costs of developing your own remote update image, driver and/or update application. The MEV remote system update solution is an out of the box complete PCIe solution including hardware, software device driver, application software and a fully documented software development kit to facilitate integration into your product's software.

The different PCIe devices can be completely unrelated and can have different hardware peripheral interfaces. The user PCIe device need not have the same resources, Vendor ID, hardware interface as the "MEV Altera Cyclone IV PCIe EPCS update device" or as any previous version of the user FPGA logic.

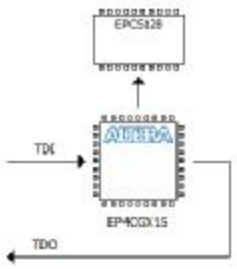
MEV RSU can be deployed onto the Altera Cyclone Development boards allowing you to accelerate your product development. This means integration of the Remote Update Solution into your software can start before your own hardware is ready.

You can also use the supplied MEV Altera Cyclone generic driver and software development kit to help prove your own FPGA design.

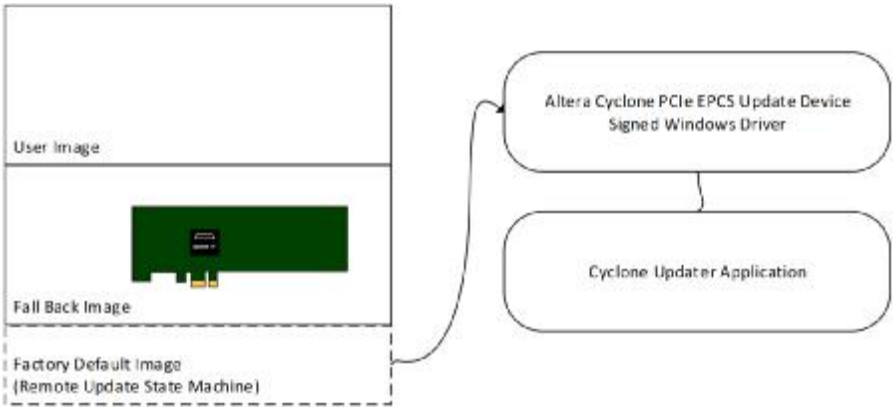
MEV offer UK based training and support for integration of the solution into your own design.

How does remote update Work?

Altera FPGAs can be configured to load their logic design from an inexpensive EPCS serial flash memory. Normally in local configuration mode the user logic design simply read from the start of the EPCS flash.



In Altera's remote update solution there are two or more configuration images. A factory default logic design and one or more user logic designs. The factory default logic and the user logic are completely independent of each other and reside in different parts of the EPCS flash. The factory default image is at the start of the EPCS flash and the user logic is at different, known, offsets.



To use the Altera Remote update solution both the factory default design and the user designs need to include a special dedicated hardware IP block provided by Altera called the Remote Update IP. They also need to be built in remote configuration mode. This allows the designs to access the embedded FPGA features that are designed to facilitate remote update.

Altera's Cyclone remote update system first loads the factory default image. This image then chooses to load the user image. If the user image fails to operate correctly the system reverts back to the factory default image.

With MEV_RSU if the user image fails to load the Remote Update Logic instantiates the "MEV Altera Cyclone IV PCIe EPCS update" device allowing the flash to be reprogrammed.

Why can't this just be done with Altera's CvP?

Altera have introduced a new technology called Configuration via Protocol (CvP). This can be used to segment your design into a periphery and core partition where the periphery is loaded from flash and the core from an RBF file via the driver.

CvP was introduced by Altera to facilitate implementation large FPGA PCIe devices. For large devices it is possible that the device load time so long that the FPGA cannot be instantiated fast enough to meet the PCIe bus set up

CvP can in theory be combined with Altera's partial reconfiguration technology to allow you to change the RBF loaded by the driver to target different core logic at your PCIe device.
There are a number of disadvantages of using this when compared to MEV RSU

- The partial reconfiguration technology is subject to additional license costs
- The original user FPGA and field updates need to share exactly the same peripheral logic. Only the core logic can be varied. Anything connecting to IO pins is locked down and cannot be changed. This appears to extend to all QSYS elements of the designs too!
- The process of separating the Core and Peripheral logic is complex, iterative and needs to be done for each design.
- The driver that loads the RBF logic needs to be developed.

With MEV RSU

- The original user FPGA and field updates are completely and absolutely independent. User designs do not need to have anything in common at all. They can have different peripherals, PCIe resources, Vendor ID…
- There is not additional process steps needed when designing your user logic other than optionally include the Remote Update Logic Component to allow the factory default image to be loaded programmatically by writing a register in your user design .
- The drivers and user applications are provided, proven and simple to use.